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ANALYSIS OF STATIC NOISE MARGIN FOR NOVEL POWER GATED SRAM

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Abstract

Data stability is one of the important parameter of SRAM with scaling of CMOS technology. However the move to nanometer technology not only nodes has increased, but the variability in device characteristics has also increased due to large process variations. Static random access memory (SRAM) is a popular component which is used in modern microprocessors and occupies a considerable chip area. It is useful to store the data as well as read and write operation. The performance of SRAM circuit is measured with data stability and read-write SNM (Static Noise Margin). A novel power gated SRAM cell is presented in this paper with enhanced data stability and reduced leakage power. The data becomes completely isolated form bit line during read operation in new power gated SRAM. The SNM of the new power gated cell is thereby increased by 2 times in comparison to a conventional six transistor (6T) SRAM cell. The paper also covers the comparative analysis and simulation of both SRAM cell on the basis of Read Noise Margin and Write Noise Margin. The novel power gated SRAM cell has larger read and write SNM as compared to conventional 6T SRAM cell at different technologies. All results are carried out on 45nm, 32nm and 22nm CMOS technology using HSPICE simulation tool.

Keywords:

Cell Ratio, Power Gated, Read Margin, Static Noise Margin, Write Margin

1. INTRODUCTION

The most popular memory in semiconductor technology is Static Random Access Memory (SRAM) that uses to save all bits in memory cell [1]. In all processor chips, SRAM covers the significant section of the processor chip. The majority of transistors are important source of leakage in SRAM arrays, which are used in high performance system and chip [2, 3]. The leakage is the only cause of SNM degradation of SRAM circuit. Thus the low leakage SRAM circuit designs are most desirable. The degradation of data retention ability of SRAM circuit with the scaling of device dimensions and voltage is the main concern in present technology [4].

In this paper, we have calculated SNM during read and write operation for both conventional 6T SRAM and new power gated SRAM, which is called Read SNM and Write SNM respectively. Read SNM and Write SNM are related to cell ratio (CR) and pull up ratio (PR) [5]. The stability of SRAM circuit also depends on the supply voltage (V_{DD}). We scale down the technology and optimized the cell design by varying parameter such as CR, PR and voltage supply. The objective is to analyze the effect of parameter change on the read - write SNM and stability of cell [6]. The new power gated SRAM circuit technique is used to enhance the data stability and improved the SNM. Read SNM and Write SNM are analyzed and compared with new power gated SRAM and conventional 6 transistors SRAM. The technique will have capability of high data stability and low leakage current. All the results are simulated on 45nm, 32nm and 22nm CMOS technology of PTM library files using HSPICE tools. The contribution of the paper is to design novel paper gated SRAM design for 45 nm, 32 nm and 22 nm CMOS technology. The proposed SRAM design has higher read and write SNM. The circuit has also reduced leakage power with compare to standard SRAM circuit

The flow of the paper is organized as follows: Section 2 covers the basics of conventional 6T SRAM cell. The design of novel power gated circuit is discussed in section 3. The simulation results are briefly analyzed in section 4 and the conclusion is derived in section 5.

2. CONVENTIONAL 6T SRAM CELLS

The 6 Transistors SRAM cell are presented with their operation and design. The important parameter cell ratio and pull up ratio are also discussed.

2.1 6T SRAM DESIGN

The design of conventional 6T SRAM includes cell ratio and pull up ratio which have substantial effect on static noise margin. The sizing effect has reasonable consideration and exponential dependency of sub threshold current. The VTC of deep submicron devices tend to change with size due to narrow channel. These impacts depended on the technology as well as the casual SNM modeling [7]. The cell ratio (β) is determined as ratio of the size of pull down NMOS transistor of the invertors and the NMOS pass transistor [8]. The cell ratio (*CR*) impacts Read SNM and pull up ratio (*PR*) defines the write SNM of the SRAM cell. The *CR* and the *PR* of the SRAM cell are discussed below: During the read operation,

$$CR = \frac{\left(W/L\right)_{PDT}}{\left(W_3/L_3\right)_{AT}} \text{ and values are 1 to 2.5}$$

Whereas, during the write operation,

$$PR = \frac{\left(W/L\right)_{PUT}}{\left(W_4/L_4\right)_{AT}} \text{ and values lies in 3 to 4.}$$

The range of *CR* and PR must be satisfied otherwise the data will be destructed. To retain the data ability and functionality of the SRAM cells, these are trivial constraint and the sizing of transistors with these constraints is given in the Table.1. To maintain read stability, N_1 and N_2 in Fig.1 should be heavier in comparison to pass transistor N_3 and N_4. On other side, to maintain write ability, N_3 and N_4 should be heavier as compare to P_1 and P_2 [9]. These demands are satisfied with heedful transistor sizing, as defined in Fig.1.

Table.1. Size of transistors applied for simulating SRAM cells

Transistors	Size [nm]		
	45nm	32nm	22nm
P_1, P_2	180	128	88
N_1, N_2	75	56	39
N_3, N_4 (AT)	45	32	22

2.2 OPERATION OF CONVENTIONAL SIX TRANSISTORS SRAM CIRCUIT

The core cell have two cross-coupled inverters implementing the positive feedback and so the two memory nodes which hold the information of node 1 and node 2. There is a requirement of two more transistors for access for read and write operation of the circuit in different way, resultant in a more robust circuit. The transistors in this work are named pull-up transistor (PUT), pull-down transistors (PDT) and access-transistors (AT). The pull up transistors are p-type, while the pull downs and access-gates are n-type. To execute read and write operations on SRAM cell pass transistor will be on if word line is high and link up the flip-flop circuit to BL and BLB [7]. There are three standard procedures hold, read and write.

The leakage current has become the dominant part of power dissipation in the nanometer CMOS technology. In CMOS transistor there are four main dominant sources of leakage - (i) reverse biased PN junction leakage, (ii) sub threshold leakage (iii) induced gate leakage and (iv) direct tunneling of gate leakage. The current will be drawn from the power supply only during switching transition.

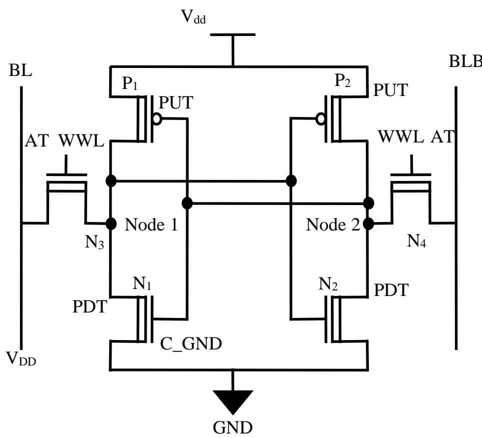

Fig.1. 6T SRAM circuit

2.2.1 *Read Operation:*

At the read operation, both BL (bit lines) and BLB (bit lines bar) are charged to VDD priory. The WL (The word line) is held during read operation. Assume that "1" is stored at node1 and implicitly a "0" is stored at node 2. If we want to read "1" than the read cycle is start by enabling two access transistors (N_3 and N_4). As a consequence data stored at node 1 and node 2 begins to transfer to the lines BL and BLB respectively. It is obvious that BLB will be discharged to the ground through N_3-N_1 and BL remains at its pre charged value.

2.2.2 *Write Operation:*

If we would wish to write logic "0" and logic "1" is already saved in the cell at node1 = 1. An accurate write operation can be assured with accurate condition of device restraints. As like to read operation, a write cycle is start by asserting WL with a little bit delay. Bit line BL and BLB are fixed to logic "0" and logic value "1" respectively to write "0" in to the cell. By providing the proper sizing of transistors the inverters to flip and alter the state of the cell.

3. NOVEL POWER GATED SRAM

Novel power gated SRAM cell is discussed in detail. The main objective of the novel power gated method is to improve the stability of data and decrease the amount of leakage current in memory circuit [10]. The schematic circuit diagram of the novel power gated SRAM circuit is demonstrated in Fig.2. The circuit consists of two back to back inverters, access transistors, read assist as well as write assist circuitry.

In order to store the data in memory cell, the high-|Vth| coupled inverters are used (formed by N_1, P_1, N_2, and P_2). The P_1 and P_2 are called as pull up transistor. N_1 and N_2 are called as pull down transistor. To control read and write operation access transistor N_3 and N_4 are used.

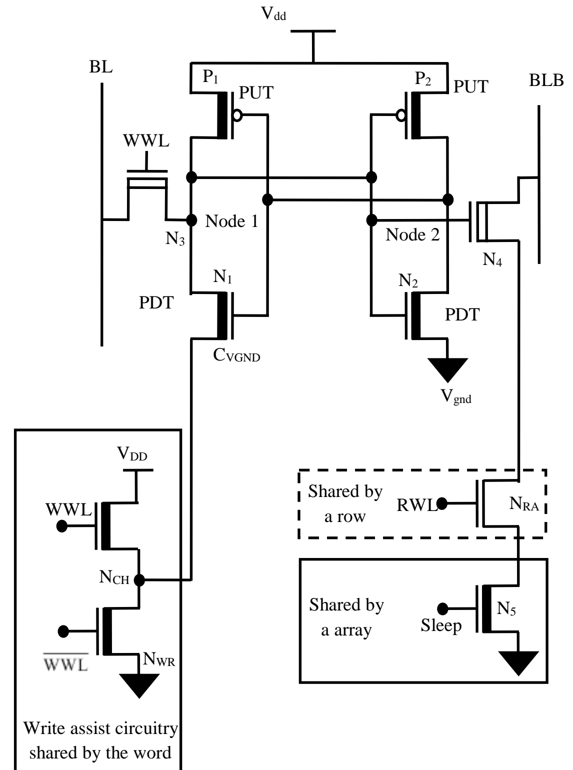

Fig.2. New power gated SRAM circuit.

The low |Vth| NRA is common in the circuit in the similar row array of the novel power gated SRAM and it is part of the read port. To decrease read bit line leakage current, a centralized high |Vth| sleep footer transistor of NMOS (N_5) is linked to all transistors (N_{RA}) which help in read assist sources in the SRAM circuit array which decreases the overall power dissipation for the SRAM circuit. In addition to write assist circuit the source of N_1

connected to NCH and NWR is helpful to improve the performance during write operation of the SRAM circuit as displayed in Fig.2. The virtual ground of the cell and the write assist circuitry are shared among the similar cells of a memory circuit. In circuit diagram the low |Vth| transistors are indicated with a thin line, whereas the channel regions of high |Vth| transistors are indicated with a thick line.

3.1 READ OPERATION

BL and BLB are charged initially to V_{DD} at starting of a single ended read operation and WL line also charged to V_{DD}. WWL line goes to V_{gnd} and SLEEP line hold at V_{DD}. Assuming that logic level “1” is to be stored at node 1 than BL is discharged by the read port which is formed by N_4, N_{RA}, and N_5. Instead of, BL is maintained at V_{DD} if a “0” is saved at node 1. During the read operation N_{WR} is turned on and NCH is cut off in the write assist circuitry. The value of C_{VGND} is held at ground level V_{gnd}. Therefore, RSNM is not reduced using the write assist circuit. After the completion of the read operation, RBL is again going to recharge at V_{DD} to prepare for next read cycle operation.

3.2 WRITE OPERATION

During the write operation, bit line BL is keep to V_{DD} if “1” is to be written on to node1 or discharged to V_{gnd} if “0” is written to on node1. To start a single ended write operation the WWL (write word line) switch to high logic value. The RWL (read word line) is held at V_{gnd} and SLEEP node is keep at V_{DD}. The data is from BL to node 1 by N_3. Transistor N_3 must be stronger as related to P_1 to successfully force logic “0” on to node 1. Similarly, to force logic “1” successfully onto node 1, N_3 is designed to be stronger with compared to transistor N_1. An assist circuitry for write operation is applied in this circuit in order to enhance the write margin. Later on during the write operation WWL is set at high, NCH held to turned on and NWR goes in cut off region. The transistor NCH charge C_{VGND} to a voltage level greater than V_{gnd}. The voltage of C_{VGND} increased N_1 become weaker because of the write margin is improved during a logic value “1” to the SRAM circuit. After the write operation is completed, BL does not require recharge to V_{DD}.

4. SIMULATION RESULTS

Read SNM and Write SNM of the 6 transistors circuit and novel power gated SRAM circuit for minimal set of the device and circuit characteristics are analyzed. Static voltage transfer characteristics for both read and write operation of the conventional 6 transistor SRAM cell and the new power gated SRAM cell are simulated at the CMOS technology of 45nm, 32nm, 22nm over voltage range from 0.8V to 1.2V.

4.1 READ STATIC NOISE MARGIN (RSNM)

Supply voltage influences the static noise margin of the SRAM circuits. It is crucial parameter for the saving supply power. SNM goes down if the applied voltage decreases. According to SNM definition the maximum value of RSNM is equal to half of the supply voltage. So that simulated vale of RSNM should be less than or equal to the half of supply voltage.

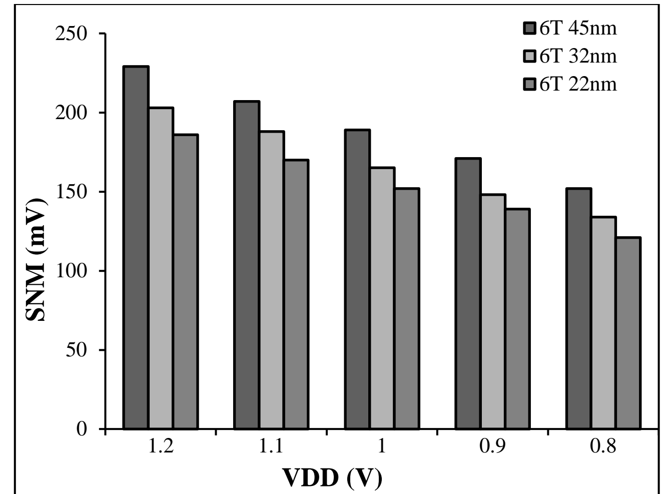

Fig.3. RSNM of 6T SRAM

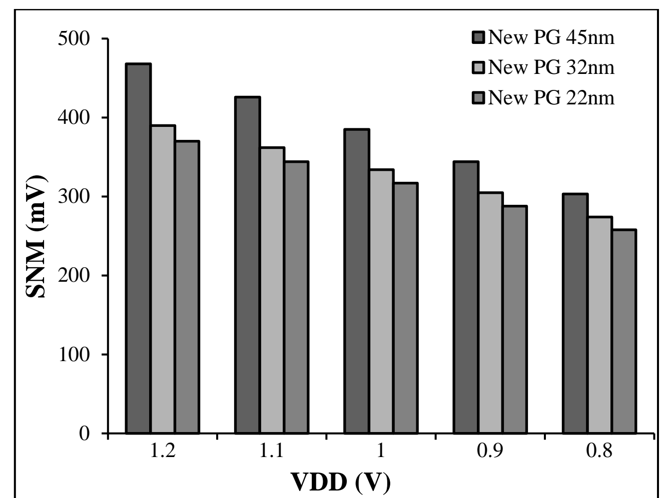

Fig.4. RSNM of Novel Power Gated SRAM

The data of the SRAM cell is most vulnerable to noise during the read operation. The read SNM of novel power gated SRAM is calculated and examined with standard 6 transistors SRAM cell. The read SNM of novel power gated SRAM cell is increased by 2 times in comparison with the standard 6 transistors SRAM cell.

The VTC of inverters of the novel power gated SRAM circuit are observed symmetric during read operation because the data is not influenced by noise when a read operation happens. On the other side, the conventional 6T SRAM has asymmetric VTC curve. Hence the data retention ability of standard 6 transistors SRAM cell is degraded. Furthermore, in new power gated SRAM cell we have high Vth due to the transition region is narrow, thereby improving the data retention stability as compared to slandered 6 transistors SRAM circuit. Read SNM are compared for both cases in Table.2.

4.2 WRITE STATIC NOISE MARGIN (WSNM)

The write SNM for storing a logic level “1” into novel power gated SRAM circuit is mainly dependent on the past or present data of the memory cell. The stored past data is likely to be same on the output of both complementary nodes. It calculates the write ability of the SRAM circuit to pull down the node where a logic

value “1” is stored to a voltage less than the switching threshold voltage of the other side inverter which stored logic level “0”. So that flipping of the state happens. WSNM is measured while writing “1”. It is observed from simulation results that there is 2 times improvement in WSNM in New power gated SRAM cell.

Table.2. RSNM of 6T SRAM and New PG

RSNM						
VDD	45nm		32nm		22nm	
	6T	New PG	6T	New PG	6T	New PG
1.2v	229	468	203	390	186	370
1.1v	207	426	188	362	170	344
1v	189	385	165	334	152	317
0.9v	171	344	148	305	139	288
0.8v	152	303	134	274	121	258

Table.3. WSNM of 6T SRAM and New PG

WSNM						
VDD	45nm		32nm		22nm	
	6T	New PG	6T	New PG	6T	New PG
1.2v	422	854	388	819	358	783
1.1v	380	780	355	745	309	711
1v	342	704	326	670	287	637
0.9v	307	625	288	590	255	558
0.8v	256	539	241	503	212	474

5. CONCLUSION

The novel power gated SRAM circuit is designed by improving the read SNM and write SNM. The leakage current is also reduced with compared to standard 6 transistors SRAM cell. The simulations for the novel power gated SRAM cell are carried out using HSPICE of 45nm, 32nm and 22nm technology. The read SNM and write SNM of the novel power gated SRAM circuit are calculated with multi threshold voltage transistors to improve the data retention ability. The novel power gated SRAM cell offers two different techniques for the data access during read and write operation. The data which is stored in a cell, is completely isolated from the bit lines, thereby the read SNM (RSNM) improved almost 2 times comparison with the standard 6 transistors SRAM cells at 45nm, 32nm and 22nm CMOS technology. Write SNM (WSNM) is also enhanced 2 times as compared to the standard 6 transistors SRAM cell. Due to that data retention ability of stored data is enhanced. RSNM and WSNM are calculated over applied VDD voltage varying from 1.2V to 0.8V. The new power gated SRAM cell has effective and significant data stability enhancement over the applied voltage variations.

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