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DFAL BASED FLEXIBLE MULTI-MODULO PRESCALER

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Abstract

The quest to have longer battery life and reduced packaging cost has been motivating factor behind developing low power circuits for different applications. Research in adiabatic logic has recently gained momentum and diode free adiabatic logic (DFAL) is one among promising variant. This paper presents a diode free adiabatic logic (DFAL) based flexible multi-modulo prescaler. It provides frequency division of 32, 33, 47, 48, 64, 65, 79 and 80 based upon the value of control signals. The functionality and performance of the proposed prescaler is investigated through TSPICE simulations by using 0.18 micron TSMC technology parameters. The performance parameters average power dissipation, time delay and PDP of the DFAL based circuit are compared with its static CMOS counterpart and a maximum power saving of 84.6% is achieved.

Keywords:

CMOS, DFAL, Dual-Modulo Prescaler, Multi-Modulo Prescaler

1. INTRODUCTION

There is immense increase in the number of components that are placed on same piece of silicon which may be attributed to aggressive and continual feature size reduction. Coupled with this is proliferation in the demand of portable consumer products and high-end circuits which culminates into shorter battery life in case the former one and requirement of cooling packages in the later. Thus the focus on low power consumption which was earlier limited to a class of integrated circuits has become part of almost every design. The research efforts have been made at various levels of VLSI design abstractions and methodologies have been worked upon. At circuit level, adiabatic logic has emerged as promising low power technique and is based on energy recycling [1-5]. Many variants of adiabatic logic namely: Two-Phase Adiabatic Static CMOS logic (2PASCL) [6], Clocked Cascadable Adiabatic Logic (CCAL) [7], Glitch Free Cascadable Adiabatic Logic (GFCAL) [8], Quasi-Static Energy Recovery logic (QSERL) [10], Positive feedback adiabatic logic (PFAL) [10], Efficient Charge Recovery Logic (ECRL) [11] and Diode Free Adiabatic Logic (DFAL) [12] are available in open literature. These styles differ in terms of the type of power supply used and path between power supply and output node.

Most of these families suffer from limitations such as large time delay, output degradation and leakage of current etc. As DFAL [12] has low power dissipation and lower PDP with respect to static CMOS and other existing adiabatic logic families, therefore it is chosen for further exploration. Different applications such as basic logic gates, full-adder, positive and negative edge triggered D-flip flop; multiplier and prescalers are developed in recent past [12-15]. A prescaler is used to divide input frequency to a lower frequency based on the division ratio (N). A flexible multi-modulo prescaler is a block which gives multiple division of frequency by making use of dual modulo prescaler. It is a constituent block of frequency synthesizers [16] and is generally employed in mobile TV, data bus synchronizer, co-prime division pre-scaler and parallel path frequency divider circuit etc. [17]. Since prescaler is a circuit which operates at higher frequency, hence power dissipation in the circuitry is very high. In this paper, DFAL based multi-modulo prescaler is proposed and its performance is examined.

In section 2, a brief description of DFAL is given. Section 3 begins with proposed DFAL-based flexible multi-modulo prescaler architecture, followed by operation of the circuit in various frequency divisions such as divide by 32, 33, 47, 48, 64, 65, 79 and 80. The proposed circuit is verified in section 4 using TSPICE simulations and performance analysis for power dissipation, time delay and power delay product has been done for each of the frequency divisions. The results of the DFAL based circuit at each frequency division are compared with the corresponding CMOS counterpart, at a frequency range of 5-100MHz. Finally, the conclusion is stated from the analysis of the results in section 5.

2. DIODE FREE ADIABATIC LOGIC (DFAL) FAMILY

The generalized block diagram of DFAL family [15] is shown in the Fig.1.

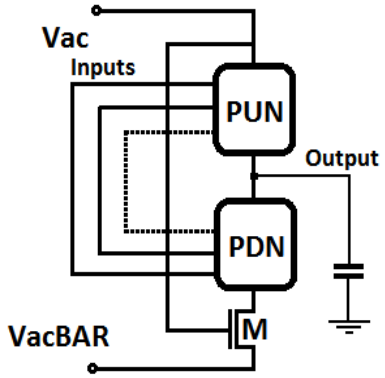


Fig.1. Generalized block diagram of DFAL family [13]

The structure is similar to CMOS logic but differ by adding an additional NMOS transistor 'M' and using split level sinusoidal power supply (V_{ac} and V_{acBAR}). It comprises of a pull-up network (PUN) and a pull-down network (PDN) for complementary operation. Transistor '*M*', driven by V_{ac}, is responsible for discharging of output and show significant power reduction by offering much smaller resistance than other adiabatic logic families to discharge the output node [7].

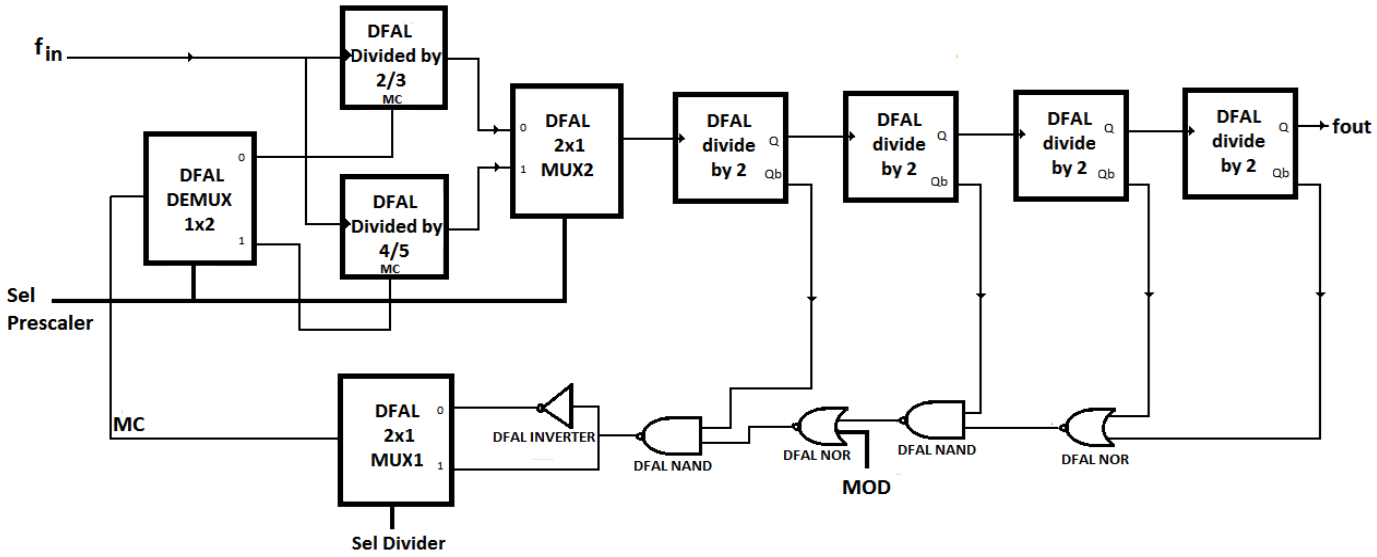


Fig.2. Proposed architecture for the flexible DFAL based multi-modulo prescaler

A DFAL gate operates in two phases namely, hold phase and the evaluation phase depending on the power supply value. In the hold phase, V_{ac} ramps down and V_{acBAR} ramps up the gate is in hold phase and no switching activity takes place, irrespective of the output voltage and inputs. Alternatively, when V_{ac} ramps up and V_{acBAR} ramps down the circuits enters evaluation phase. Depending upon the inputs the output follows the power supply signal. That is, if inputs are such that the PUN is active then the output node follows the V_{ac} signal (ramps up) otherwise for activated PDN, the output node follows the V_{acBAR} (ramps down) signal.

3. PROPOSED MULTI-MODULO PRESCALER

A prescaler is a constituent block of any communication systems. It is a circuit block used for lowering the frequency of signal (f_{in}) by factor (X). Some of the existing prescaler in DFAL family include Frequency divide-by-2, frequency divider-by-3, prescaler by 3 with 50% duty cycle and prescaler by 5 with 50% duty cycle. In this paper, a flexible multi-modulo prescaler, a major block in multi-band flexible divider in a frequency synthesizer is worked upon. The proposed architecture and the operation of the flexible multi-modulo prescaler are presented.

3.1 ARCHITECTURE

The proposed architecture for a DFAL based flexible multi-modulo prescaler circuit as shown in Fig.2. It consists of two dual-modulo prescalers i.e. 2/3 and 4/5, an asynchronous divide by 16 circuit, two multiplexers (MUX1 and MUX2), a demultiplexer (DEMUX) and few combinational gates for intermediate signal generations. There are three control signals modulo control (MOD) signal, Sel Prescaler, Sel Divider used for the selection of the divide by factor. The input signal with frequency (f_{in}) is fed to the dual-modulo prescaler block then depending upon the value of Sel prescaler and an intermediate MC control signal either 2/3 or 4/5 gets selected. The signal passes further through the asynchronous divide by 16 circuits. The intermediate signals of the divide-by-2 circuits in connection with the control signal modulo control MOD are used to generate appropriate inputs to the Sel Divider multiplexer. The output of the multiplexer then forms the MC signal used for prescalers selection. The DFAL based block diagram of the individual constituents such as dual modulo 2/3 prescaler dual modulo 4/5 prescaler and 1×2 DEMUX and 2×1 MUX are shown in Fig.3 for complete reference.

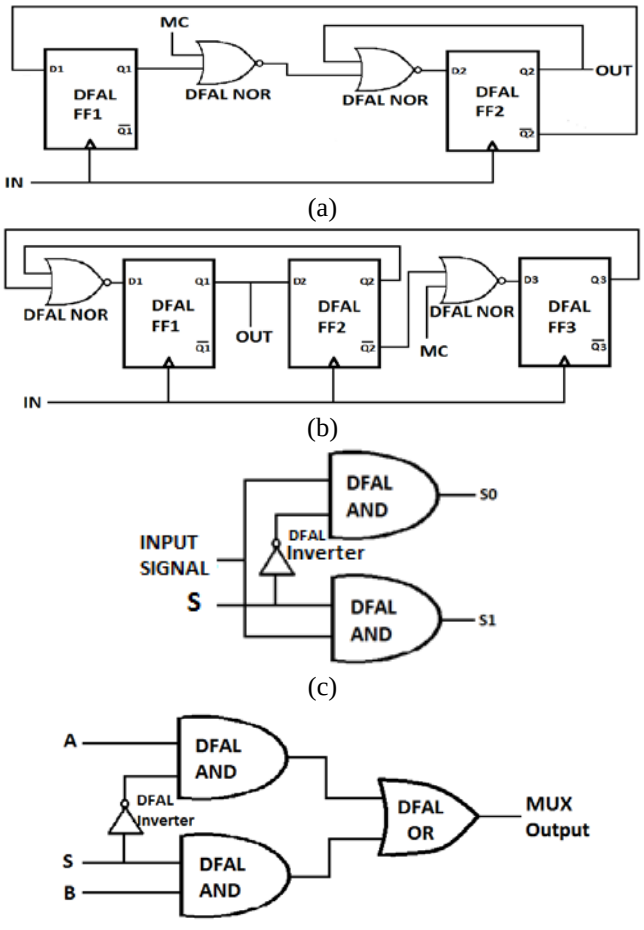


Fig.3. Block diagram of a) dual modulo 2/3 Prescaler b) dual modulo 4/5 Prescaler c) 1×2 DEMUX d) 2×1 MUX

3.2 OPERATION OF THE CIRCUIT

The proposed architecture provides frequency division factor N depending upon Sel Prescaler, Sel Divider and MOD control signals. The frequency division factor N for various combinations of control signals are enlisted in Table.1. Based on the proposed architecture, it is clear that the selection of dual modulo prescalers (2/3 and 4/5) is decided by "Sel Prescaler" and mode control (MC) signals. For Sel Prescaler = 0, the MC signal is sent to 2/3 modulo prescaler through DEMUX and the output of the 2/3 modulo prescaler is selected using MUX2 with further connects to divide by 16 block and gives frequency division at $f_{out.}$ Similarly, for Sel Prescaler = 1, the 4/5 modulo prescaler path is enabled i.e. the MC signal is given to 4/5 prescaler using DEMUX and the output of the 4/5 prescaler connects to the divide by 16 block. It is evident now that the generation of the appropriate MC signal is thus essential. The Sel Divider and MOD control signals along with the combinational gates generates the MC signal. An in-depth discussion on its generation for all the combination of the control signals is presented further.

Table.1. Frequency division in accordance to Selection Control signal for proposed circuit

SEL Prescaler	SEL Divider	MOD	Frequency division factor N
0	1	1	32
0	1	0	33
0	0	0	47
0	0	1	48
1	1	1	64
1	1	0	65
1	0	0	79
1	0	1	80

3.2.1 Case 1: Select Prescaler = 0, SEL Divider = 1, MOD = 1

When MOD is at logic 1, the NOR gate gives logic 0 irrespective of its second input. This logic 0 signal when passed to NAND gate gives logic 1 always and the MUX1 gets two signals either logic 1 or 0 at its input. Now if "SEL Divider" signal = 1, then the MUX1 will select logic 1 and set MC = 1. Now this MC control signal will enable divide by 2 out of 2/3. After the selection of divide by 2 modulo in the asynchronous block of divide by 16, it will give a resultant frequency division of 32 at the f_{out}. A pictorial representation of the selection is shown in Fig.4 where continuous line signifies that the block is in use while the dotted line denotes non usage.

3.2.2 Case 2: Select Prescaler = 0, SEL Divider = 1, MOD = 0

If MOD is logic 0 then the combinational part of the proposed circuit is enabled. Now "Sel Divider" = 1 enables the input of the MUX1 coming out from the NAND gate. This give rise to frequency division of 33 though the dual modulo 2/3 prescaler.

3.2.3 Case 3: Select Prescaler = 0, SEL Divider = 0, MOD = 1

When MOD is logic 1 the NOR gate gives logic 0 irrespective of its second input. This logic 0 signal when passed to NAND gate gives logic 1 always and the MUX1 gets two signals either logic 1 or 0 at its input. Now if "Sel Divider" signal=0, then the MUX1 will select logic 0 and set MC = 0. Now this MC control signal will enable divide by 3 out of 2/3. After the selection of divide by 3, modulus the asynchronous block of divide by 16 will give a resultant frequency division of 48 at the f_{out}.

3.2.4 Case 4: Select Prescaler = 0, SEL Divider = 0, MOD = 0

If MOD is logic 0 then the combinational part of the proposed circuit is enabled. Now "Sel Divider" = 1 enables the input of the MUX1 coming out from the NAND gate. This will give rise to frequency division of 47 though the dual modulo 2/3 prescaler.

3.2.5 Case 5: Select Prescaler = 1, SEL Divider = 1, MOD = 1

When MOD is logic 1 the NOR gate gives logic 0 irrespective of its second input. This logic 0 signal when passed to NAND gate gives logic 1 always and the MUX1 gets two signals either logic 1 or 0 at its input. Now if "Sel Divider" signal=1, then the MUX1 will select logic 1 and set MC=1. Now this MC control signal will enable divide by 4 out of 4/5. After the selection of divide by 4, modulus the asynchronous block of divide by 16 will give a resultant frequency division of 64 at the f_{out}.

3.2.6 Case 6: Select Prescaler = 1, SEL Divider = 1, MOD = 0

If MOD is logic 0 then the combinational part of the proposed circuit is enabled. Now "Sel Divider" = 1 enables the input of the MUX1 coming out from the NAND gate. This will give rise to frequency division of 65 though the dual modulo 2/3 prescaler.

3.2.7 Case 7: Select Prescaler = 1, SEL Divider = 0, MOD = 1

When MOD is logic 1 the NOR gate gives logic 0 irrespective of its second input. This logic 0 signal when passed to NAND gate gives logic 1 always and the MUX1 gets two signals either logic 1 or 0 at its input. Now if "Sel Divider" signal=0, then the MUX1 will select logic 0 and set MC=0. Now this MC control signal will enable divide by 5 out of 4/5. After the selection of divide by 5, modulus the asynchronous block of divide by 16 will give a resultant frequency division of 80 at the f_{out}.

3.2.8 Case 8: Select Prescaler = 1, SEL Divider = 0, MOD = 0

If MOD is logic 0 then the combinational part of the proposed circuit is enabled. Now "Sel Divider" = 1 enables the input of the MUX1 coming out from the NAND gate. This will give rise to frequency division of 79.

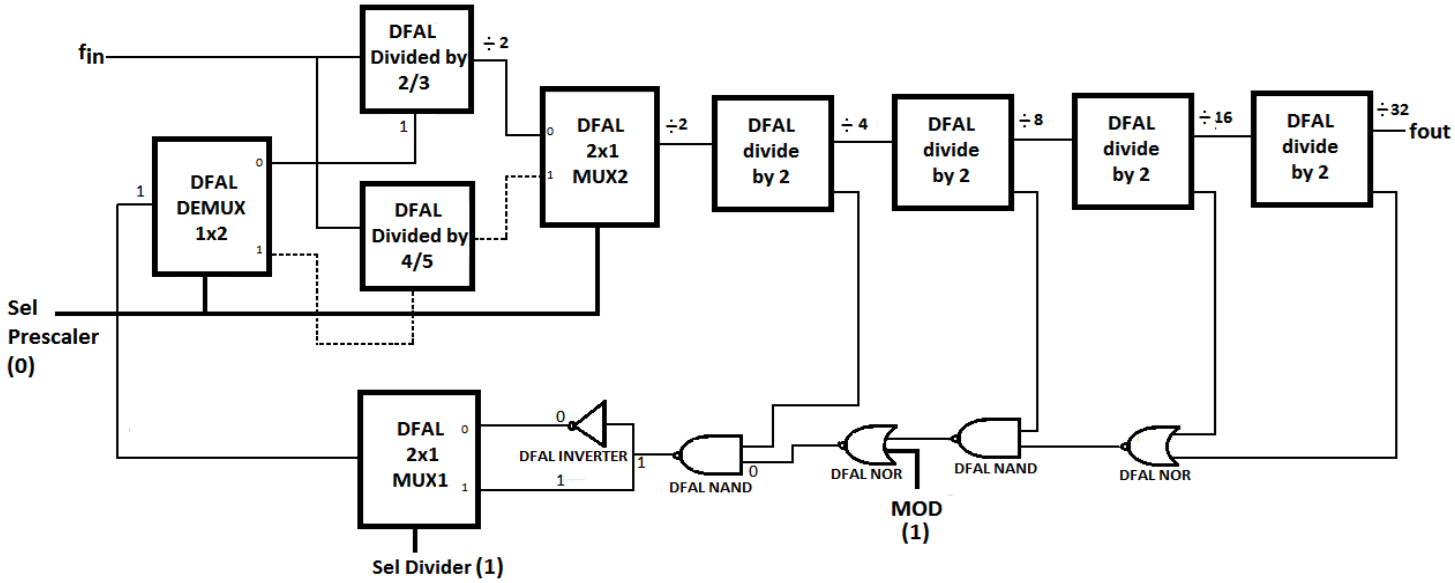


Fig.4. Proposed architecture operating as Divide by 32 prescaler under case 1

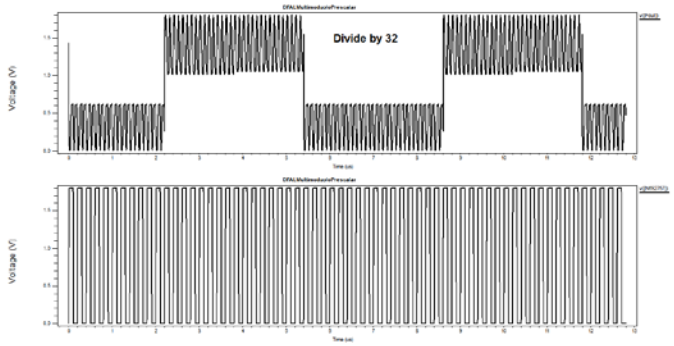
4. SIMULATION RESULTS

The functionality of the proposed flexible multi-modulo prescaler is verified for all division factors through TSPICE simulations using 180 nm CMOS technology parameters. The performance of the proposed DFAL prescalers is compared with its CMOS counterpart in terms of power dissipation, time delay and power delay product (PDP) for varying input frequency ranging from 5MHz to 80MHz. For DFAL circuits, the input frequency is kept half of supply clock frequency. Load capacitance and transistor aspect ratio of 100 fF and 540 nm/180 nm respectively are taken in simulations for both the styles. The section first functionally verifies the feasibility of the proposed flexible multi-modulo prescaler and then presents the simulation results for the performance evaluation.

The results for proposed circuits are compared with the results of its CMOS counterpart in the subsections below for all the different frequency divisions i.e. 32, 33, 47, 48, 64, 65, 79 and 80.

4.1 FUNCTIONAL VERIFICATION OF THE PROPOSED ARCHITECTURE

The proposed DFAL based flexible multi-modulo prescaler is configured for different frequency division factor i.e. 32, 33, 47, 48, 64, 65, 79 and 80 according to Table.1. For operation as divide by 32 prescaler (case 1), the control signals Sel Prescaler, Sel Divider and MOD logic levels are set to low, high and high respectively. The output waveform for the first two divide by 32 cycles of the proposed divide by 32 prescaler is shown in Fig.5(a). The waveforms corresponding to the different cases II-case VIII are shown in Fig.5(b)-Fig.5(h). It can be observed that the proposed DFAL based flexible multi-modulo prescaler is able to conform to the required functionality. Similar waveforms were obtained from the CMOS based prescalers and are omitted.



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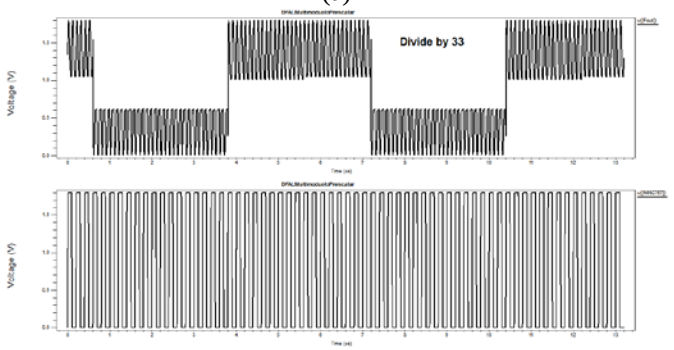

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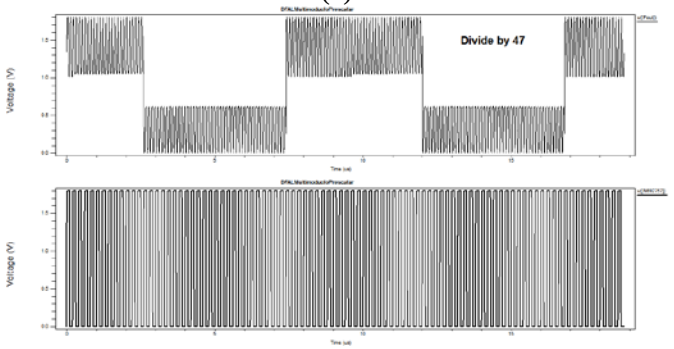

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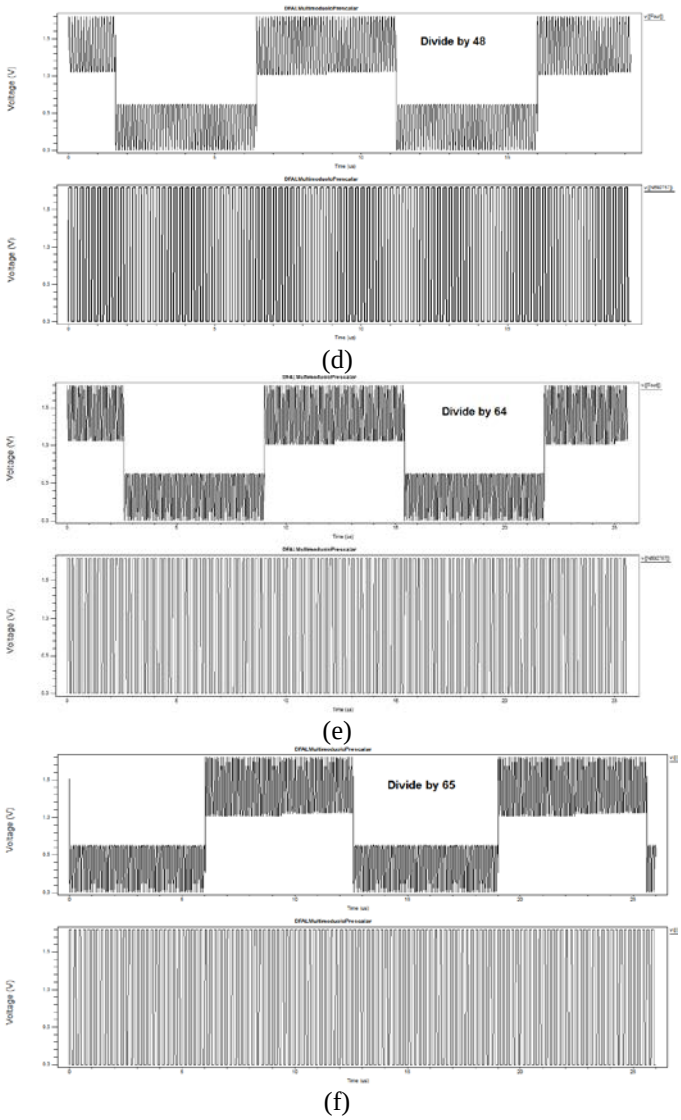


Fig.5. Simulation waveforms of Prescalers a) case 1: Divide by 32 b) case 2: Divide by 33 c) case 3: Divide by 47 d) case 4: Divide by 48 e) case 5: Divide by 64 f) case 6: Divide by 65 g) case 7: Divide by 79 h) case 8: Divide by 80

4.2 PERFORMANCE EVALUATION

The performance of the proposed DFAL based flexible multi-modulo prescaler is evaluated in terms of power, delay and PDP. A complete listing of the values of these parameters for all the cases of DFAL and CMOS based prescalers are summarized in Table.2.

Table.2. Summary of Simulation Results

Frequency / Style	5 MHz	10 MHz	16 MHz	25 MHz	50 MHz	62.5 MHz	100 MHz	Max % improvement w.r.t. CMOS
Divide-by-32								
Power Dissipation (uW)								
Static CMOS	8.66	10.84	13.48	17.48	28.27	34.83	40.71	80.48%
DFAL	1.69	3.26	5.26	8.32	18.66	24.75	33.39	
Time Delay (ns)								
Static CMOS	1.00	1.25	1.37	1.37	1.36	1.36	1.37	
DFAL	2.98	2.60	2.36	2.13	1.81	1.75	1.70	
PDP (fJ)								
Static CMOS	8.66	13.55	18.46	23.94	38.44	47.36	55.77	41.92%
DFAL	5.03	8.47	12.41	17.72	33.77	43.31	56.76	
Divide-by-33								
Power Dissipation (uW)								
Static CMOS	8.74	10.89	13.51	17.53	28.33	34.88	40.84	80.89%
DFAL	1.67	3.23	5.22	8.26	18.55	24.62	33.22	

Time Delay (ns)								
Static CMOS	1.03	1.26	1.32	1.37	1.37	1.37	1.36	
DFAL	2.97	2.62	2.37	2.12	1.82	1.74	1.70	
PDP (fJ)								
Static CMOS	9.00	13.72	17.83	24.01	38.81	47.78	55.54	45%
DFAL	4.95	8.46	12.37	17.51	33.76	42.83	56.47	
Divide-by-48								
Power Dissipation (uW)								
Static CMOS	8.32	10.14	12.42	15.73	24.54	30.01	35.70	82.81%
DFAL	1.43	2.72	4.38	6.89	16.08	21.30	28.70	
Time Delay (ns)								
Static CMOS	1.00	1.21	1.32	1.37	1.37	1.36	1.36	
DFAL	2.95	2.64	2.38	2.15	1.81	1.74	1.70	
PDP (fJ)								
Static CMOS	8.32	12.26	16.39	21.55	33.61	40.81	48.55	49.40%
DFAL	4.21	7.18	10.42	14.81	29.10	27.06	48.79	
Divide-by-47								
Power Dissipation (uW)								
Static CMOS	8.30	9.88	12.34	15.67	24.66	30.19	35.96	82.41%
DFAL	1.46	2.77	4.46	7.03	16.39	21.71	29.31	
Time Delay (ns)								
Static CMOS	1.00	1.30	1.33	1.36	1.37	1.36	1.37	
DFAL	3.00	2.67	2.37	2.13	1.81	1.74	1.72	
PDP (fJ)								
Static CMOS	8.30	12.84	16.41	21.31	33.78	41.05	49.26	47.29%
DFAL	4.38	7.39	10.57	14.97	29.66	37.77	50.41	
Divide-by-64								
Power Dissipation (uW)								
Static CMOS	8.54	9.67	11.61	14.64	22.60	27.74	32.92	84.31%
DFAL	1.34	2.47	3.96	6.29	14.88	19.72	26.57	
Time Delay (ns)								
Static CMOS	0.86	1.25	1.32	1.36	1.36	1.36	1.36	
DFAL	2.94	2.63	2.35	2.13	1.81	1.74	1.69	
PDP (fJ)								
Static CMOS	7.34	12.08	15.32	19.91	30.73	37.72	44.77	46.46%
DFAL	3.93	6.49	9.30	13.39	26.93	34.31	44.90	
Divide-by-65								
Power Dissipation (uW)								
Static CMOS	8.60	9.67	11.69	14.75	22.75	28.09	33.20	84.19%
DFAL	1.36	2.50	4.00	6.34	15.01	19.89	26.81	
Time Delay (ns)								
Static CMOS	0.93	1.25	1.32	1.37	1.37	1.36	1.36	
DFAL	2.97	2.63	2.36	2.13	1.82	1.73	1.69	
PDP (fJ)								
Static CMOS	7.99	12.08	15.43	20.20	31.16	38.20	45.15	49.56%
DFAL	4.03	6.57	9.44	13.50	27.31	34.40	45.30	

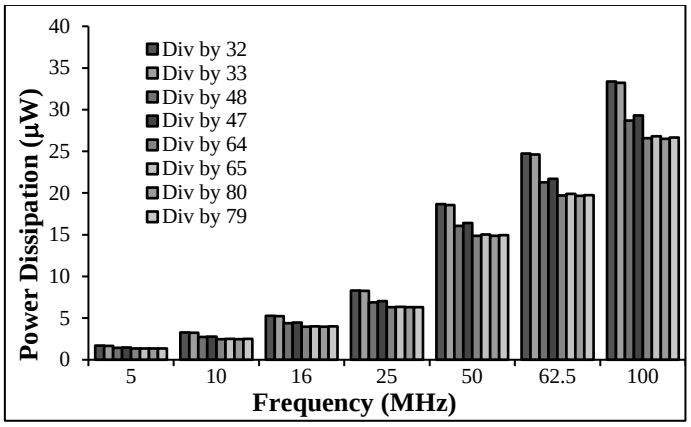
Divide-by-80								
Power Dissipation (uW)								
Static CMOS	8.44	9.67	11.52	14.51	22.43	27.55	32.62	84.12%
DFAL	1.34	2.48	3.98	6.29	14.86	19.66	26.49	
Time Delay (ns)								
Static CMOS	0.83	1.23	1.33	1.36	1.37	1.36	1.36	
DFAL	2.94	2.61	2.36	2.16	1.82	1.74	1.68	
PDP (fJ)								
Static CMOS	7.00	11.89	15.32	19.73	30.72	37.46	44.36	43.86%
DFAL	3.93	6.47	9.39	13.58	27.04	34.20	44.50	
Divide-by-79								
Power Dissipation (uW)								
Static CMOS	8.70	9.88	11.88	15.03	22.83	28.47	33.64	84.60%
DFAL	1.34	2.49	4.00	6.31	14.93	19.75	26.64	
Time Delay (ns)								
Static CMOS	0.94	1.25	1.32	1.36	1.37	1.36	1.36	
DFAL	2.95	2.60	2.35	2.10	1.81	1.75	1.73	
PDP (fJ)								
Static CMOS	8.17	12.35	15.68	20.44	31.27	38.71	45.75	51.65%
DFAL	3.95	6.47	9.40	13.25	27.02	34.56	46.08	

The simulated results can be analyzed as,

1. The DFAL based flexible multi-modulo prescaler show lower power values in comparison to CMOS based. A maximum power saving of 84.6 % w.r.t CMOS based prescaler is achieved with DFAL based prescaler.
2. An increased in the delay values of the proposed DFAL prescaler is achieved w.r.t CMOS based prescaler. This behavior matches to the basic nature of adiabatic circuits of achieving low power operation by having large delay values.
3. The DFAL based prescaler outperforms in terms of PDP values for all the measured frequencies. This indicates that the power saving is more than speed degradation.

To study the behavior of the proposed DFAL based prescaler at different frequencies a bar graph representation is plotted in Fig.6. The analysis can be summarized as:

1. There is a rising trend in the power consumption of the prescalers w. r. t. increasing input frequency whereas a falling trend is observed for the delay values.
2. The PDP curve show an increasing trend w. r. t. input frequency as the increase in power is much more pronounce than the reduction in the delay values.
3. The delay values of the prescaler configured for all the cases show almost same delay values at a particular input frequency.



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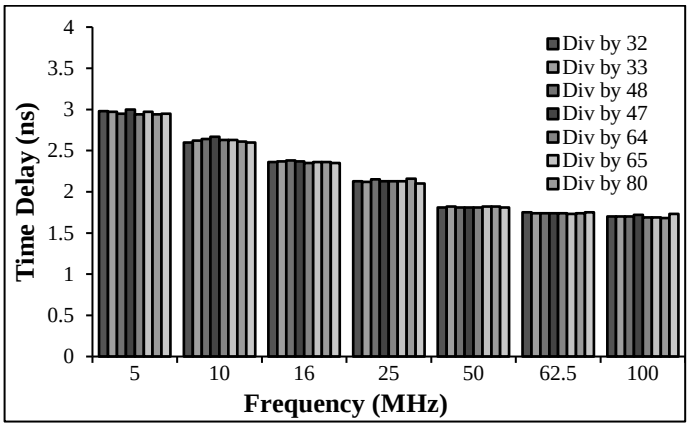

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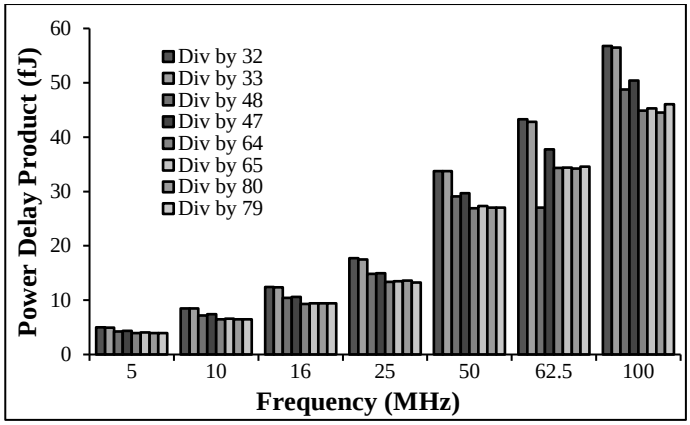

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Fig.6. Performance evaluation of the DFAL multi-modulo prescaler configured for all at different frequency

5. CONCLUSION

A new DFAL based architecture for flexible multi-modulo prescaler has been presented in this paper which is a constituent block of frequency synthesizer. The proposed architecture shows better performance for various frequency divisions i.e. 32, 33, 47, 48, 64, 65, 79 and 80 with respect to static CMOS in terms of PDP and power dissipation under varying clock frequency. From the analysis of power dissipation results, DFAL based flexible multi–modulo prescaler shows average maximum power dissipation reduction of 84.6% among various frequency divisions.

The detailed study of the proposed circuit shows that the DFAL based circuit surpasses the CMOS based industry standard in terms of lower power dissipation. Since there is a significant reduction in power, the proposed circuit can be used in many applications of frequency synthesizers such as mobile phones, GPS systems walkie-talkies, satellite receivers with a much better performance and higher efficiency. Also, since the proposed architecture can provide multiple frequency synthesis, it may be useful in different scenarios for different applications which require a specific frequency synthesis. Hence DFAL can be a suitable alternative of conventional CMOS for low power in many existing and future applications.

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