ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2017.0058

DESIGN AND ANALYSIS OF AN EFFICIENT FULL ADDER USING SYSTEMATIC CELL DESIGN METHODOLOGY

Jyothish Chandran G, Anila Susan George and Anu Raj
Department of Electronics and Communication Engineering, Saintgits College of Engineering, India

Abstract

In this paper, a high performance and low power full adder using Systematic Cell Design Methodology (SCDM) is explained. The design is initially executed for 1 bit and afterward reached out to 4 bit too. The circuit was implemented using Mentor Graphics tools at 180 nm technology. The performance parameters like average propagation delay, average power and Power Delay Product (PDP) are compared with existing hybrid adders like SRCPL adder and DPL adder. The proposed adder has less number of transistors in the critical path leading to less propagation delay. The utilization of transmission gate all through the design guarantees high driving ability and full voltage swing at the output. The proposed adder is observed to work productively when compared with different adders in terms of average power, average propagation delay and PDP. The Schematic Driven Layout of the proposed adder is obtained using Mentor Graphics IC station and the physical verifications are done using Calibre tool.

Keywords:

Three Input XOR/XNOR, Systematic Cell Design Methodology, Transmission Gate, Full Adder, Low Power High Performance

1. INTRODUCTION

The development of generation has multiplied the call for low power electronic systems. For the reason that those low power structures provide long lasting battery operation, they may be used for portable applications. However, there is a requirement for high speed designs in order that efficient operation at high frequencies will be ensured. Alas, to reduce the power of a circuit one should normally compromise on its speed, when you consider that lower power translates into smaller current which could in the end cause a slower circuit. As an end result a useful metric utilized in such instances is the Power Delay Product (PDP) which can be used to represent the overall performance of a system. The Power-Delay Product (PDP) refers to the quantity of energy spent throughout the conclusion of a determined task, and stands as the more truthful performance metric when examining optimizations of a module designed and tested using completely different technologies, operational frequencies, and scenarios [3].

In the majority of systems, the adder is an element of the vital path that governs the general performance of the system. It is primarily employed in lot of VLSI systems like microprocessors and application specific DSP design. Additionally to its main task, that is, adding 2 numbers, it is employed in several alternative helpful operations like subtraction, multiplication, address calculation, etc. All these operations are realized by complex system of transistors. The critical path consists of transistors that produce the maximum time-delay in the output signal. The conduct of transistors inside the critical path basically determines the overall performance of the entire system. Thus the performance of the adders can be considered as extremely significant for VLSI systems.

This paper proposes a full adder designed using systematic cell design methodology. A carry/carry-inverse block is designed additionally to the three input XOR/XNOR structure to create the ultimate full adder. The entire design is done using transmission gates which offer full output voltage swing, increase circuit driving capability and eliminate the requirement for optimization techniques. The resultant adder is compared with already existing hybrid adders like DPL (Double Pass-transistor Logic) adder and SRCPL (Swing restored Complimentary Pass transistor Logic) adder [3].The proposed adder is symmetric and is relatively PDP efficient. A four bit structure of the proposed adder is developed to investigate its performance in real environment. The whole circuit is drawn using Mentor Graphics Pyxis tool and simulated using Eldo simulator. The Schematic Driven Layout (SDL) of the proposed adder is obtained using Mentor Graphics IC station and the physical verifications are carried out using Calibre tool.

2. LITERATURE SURVEY

Many papers have been published so far which compete in designing better circuits [1][2][3]. Though the circuits depend on creative design ideas, they do not follow a systematic approach. As a result such circuits [3] suffer from certain drawbacks.

- The logic styles incorporated in such circuits lack complete voltage swing in some internal nodes thereby leading to static power dissipation.
- Most of the circuits cannot sustain low voltage operation due to output signal degradation.
- Dynamic power consumption prevails for non-balanced propagation delays, which thereby result to glitches at the output.

The above mentioned drawbacks could be solved by following a well organized design methodology. Cell Design Methodology has been introduced [4][5] which is used to design limited functions. This Cell Design Methodology is later improved to a Systematic Cell Design Methodology (SCDM) for the design of a three input XOR/XNOR structure [6]. The methodology systematically generates Elementary Basic Cell (EBC) by using Binary Decision Diagram (BDD) and wisely chooses the circuit components based on a specific target [6]. The resultant XOR/XNOR structure was found to have full swing and fairly balanced output. The design of the XOR/XNOR structure using SCDM is explained in the next section.

3. SYSTEMATIC CELL DESIGN METHODOLOGY

The SCDM aims in attaining the target by following a sequence of steps in a systematic way. The target considered is Power-Delay Product (PDP). The main design goals of SCDM are

generating balanced outputs, power-ground free and symmetric structure and less number of transistors in the critical path [6]. The methodology mainly involves Elementary Basic Cell (EBC) generation and wise selection of mechanisms and cells. The EBC generation of a 3 input XOR/XNOR follows a sequence of steps.

1. Representation of Binary Decision Tree (BDT) of three input XOR/XNOR structure.
2. Application of reduction rules
3. Substitution of $\overline{Y}$ for 0 and Y for 1
4. Disjointing simplified symbol

The BDT of three inputs XOR/XNOR is initially represented using seven 2×1 MUX blocks were *A*, *B* and *C* are the select lines which control the inputs at each corresponding level. A_1, A_2, A_3, A_4, B_1, B_2 and C_1 are the outputs of the respective MUX blocks as shown in Fig.1. The inputs and outputs of each block is shown in the Table.1.

Table.1. Inputs and outputs of MUX blocks

Select lines			Outputs of each MUX block						
A	**B**	**C**	**A_1**	**A_2**	**A_3**	**A_4**	**B_1**	**B_2**	**C_1**
0	0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1	1
0	1	0	0	1	1	0	1	0	1
0	1	1	0	1	1	0	1	0	0
1	0	0	1	0	0	1	1	0	1
1	0	1	1	0	0	1	1	0	0
1	1	0	1	0	0	1	0	1	0
1	1	1	1	0	0	1	0	1	1

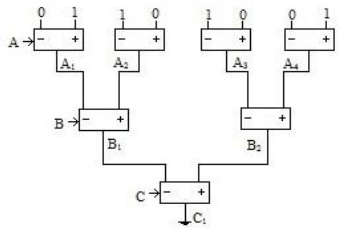

Fig.1. BDT representation of 3 input XOR/XNOR [6]

The BDT is then simplified by the application of reduction rules as shown in Fig.2 which include elimination, merging and coupling rules. The coupling rule aim in obtaining all possible equivalent trees by interchanging the order of controls.

Then the inputs '1' and '0' are replaced by *Y* and $\overline{Y}$ respectively. At last each block is disjointed into individual units as shown in Fig.3, the plus sign with *X* input control and the negative sign with $\overline{X}$ input control.

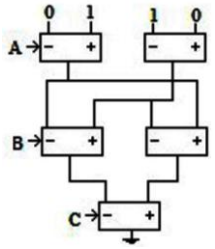

Fig.2. Applying reduction rules [6]

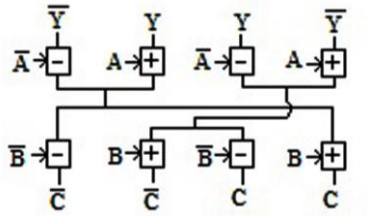

Fig.3. Substitution and disjointing [6]

The EBC thus extracted shown in Fig.4 has eight elements leading to two outputs.

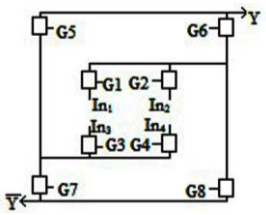

Fig.4. EBC [6]

The pins of the central section (In1-In4 and G1-G4) refer to A or B, or their complements while that of external section G5-G8 refer to C or its compliment.

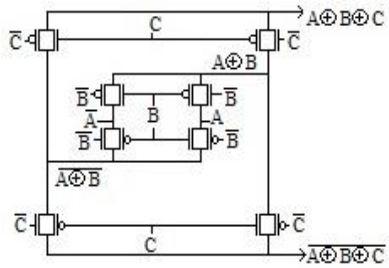

Fig.5. Three input XOR/XNOR structure [6]

The three input XOR/XNOR structure shown in Fig.5 is finally obtained by replacing the elements with transmission gates and the control inputs with respective input signals.

3.1 PROPOSED ADDER

The three input XOR/XNOR structure is extended to a full adder by the addition of carry/carry-inverse block. The carry/carry-inverse block design is deducted by analyzing the truth table of a full adder. If the inputs *A* and *B* are equal, *Carry=B*, $\overline{Carry} = \overline{B}$; else input *Carry* = *C*, $\overline{Carry} = \overline{C}$.

$$Carry = B(A \odot B) + C(A \oplus B) \quad (1)$$

$$\overline{Carry} = \bar{B}(A \odot B) + \bar{C}(A \oplus B) \quad (2)$$

The whole design is done using transmission gates which provide full voltage swing at the output.

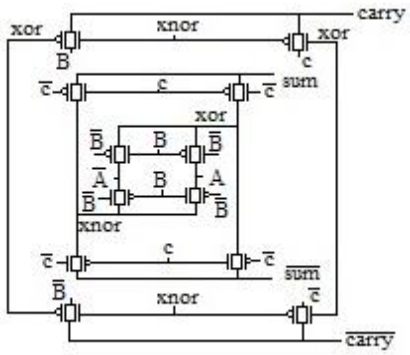

Fig.6. Circuit diagram of proposed full adder

The resulting circuit is symmetric, power-ground free and possesses balanced outputs. The proposed full adder structure is shown in Fig.6.

4. SIMULATION RESULTS

The proposed adder is set up using Mentor Graphics Pyxis tool and the simulation is done using Mentor Graphics ELDO tool based on TSMC 0.18µm technology. The propagation delay is measured between *C*, Carry and Carry-inverse respectively keeping inputs *A* and *B* constant. The average propagation delay thus obtained is 23ps and the average power dissipation is 475.153pW. The proposed adder is then compared with two existing hybrid adders, SRCPL adder and DPL adder [3] to evaluate its performance based on average power, average delay and PDP. The proposed adder is found to have less PDP compared to other two adders. The corresponding results are shown in Table.2.

Table.2. Simulation results in 180nm technology

Type of adder	Average Power (pW)	Average Delay (ps)	Power-Delay Product (aJ)
DPL Adder	1284.200	52.918	0.067
SRCPL Adder	930.200	54.349	0.050
Proposed Adder	475.153	23.00	0.010

In real time conditions, one bit adder might not work properly since the inputs are not fed directly. Instead they are fed by the outputs of the preceding stages. To investigate the success of the proposed adder throughout its actual use in VLSI applications, a simulation test bench is set up as shown in Fig.7.

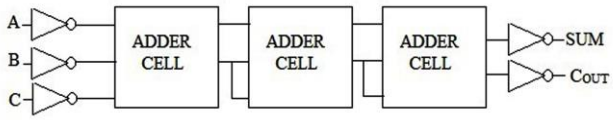

Fig.7.Simulation Test Bench

Table.3. Simulation Results in 180nm technology using simulation test bench

Type of adder	Average Power (nW)	Average Delay (ps)	Power-Delay Product (aJ)
DPL Adder	3.9712	2427.6	9.640
SRCPL Adder	3.0132	1596.7	4.811
Proposed Adder	1.4701	378.364	0.556

To make a realistic environment, inverters are added at the input and output of the test bench. The inverters at the input add the impact of input capacitance whereas that at the output ensures proper loading conditions. The test bench is applied to the proposed adder, SRCPL adder and DPL adder. The results of the adders using simulation test bench is shown in Table.3. It is observed that the proposed adder is relatively efficient in terms of average power, average delay and PDP.

4.1 PERFORMANCE OF FOUR BIT ADDER

A 4 bit ripple carry adder [Fig.8] is implemented as an extension to the proposed 1 bit full adder.

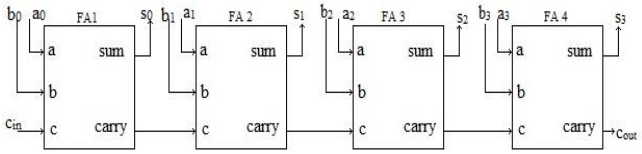

Fig.8. Four bit ripple carry adder using 1 bit proposed adder with true outputs

The carry propagates all the way to the last adder in the ripple carry adder structure. The performance evaluation is carried out using 180nm technology. The 4 bit structure of the proposed adder is compared with four bit CMOS adder.

Table.4.Simulation results of 4 bit adders in 180nm technology

Type of adder	Average Power (nW)	Average Propagation Delay (ps)	Power-Delay Product (aJ)
4 bit CMOS adder	3.8072	50.899	0.193
4 bit Proposed Adder	1.4578	53.820	0.078

It is observed [Table.4] that the four bit structure of proposed adder is efficient compared to the four bit CMOS adder in terms of average power, average carry propagation delay and PDP.

4.2 LAYOUT AND PHYSICAL VERIFICATION

The layout of the proposed adder has been obtained using Mentor Graphics IC station as shown in Fig.9.

The green structures with red polysilicon lines are the PMOS and NMOS transistors. The blue lines show the metal layers namely metal 1. The inputs and outputs are shown using the input and output ports. Polysilicon contacts are provided between metal and polysilicon interconnections. VDD supply and ground are shown by green and yellow horizontal metal lines respectively which are placed 120λ apart.

In order to verify the design rule violations with the placement of instances, DRC was run and verified that the design contain no errors. After verifying the design rules with DRC, Layout Versus Schematic (LVS) was used to check whether the layout matches with the schematic.

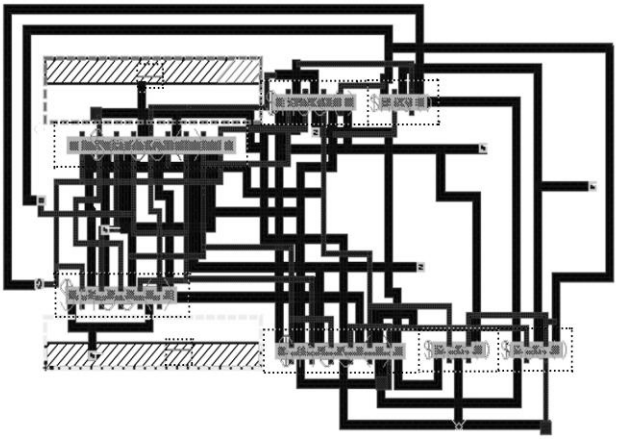

Fig.9. Schematic Driven Layout of proposed adder

5. CONCLUSION

In this paper a 1 bit full adder is proposed utilizing SCDM which is later extended to 4 bit ripple carry adder. The simulation was done using Mentor Graphics Pyxis and Eldo tool with 180nm technology and compared with existing hybrid adders like DPL adder and SRCPL adder. The simulation results prove that the one bit proposed adder offer PDP optimization up to 82% when compared to SRCPL and DPL hybrid adders. The Schematic Driven Layout (SDL) of the proposed adder was obtained using Mentor Graphics IC station and the physical verifications were carried out using Calibre tool. The use of SCDM as the design methodology ensures a symmetric and power-ground free structure.

REFERENCES

[1] C.H. Chang, J. Gu and M. Zhang, "A Review of 0.18-µm Full Adder Performances for Tree Structured Arithmetic Circuits", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 13, No. 6, pp. 686-695, 2005.

[2] Sumeer Goel, Ashok Kumar and Magdy A. Bayoumi, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 14, No. 12, pp. 1309-1321, 2006.

[3] Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 19, No. 4, pp. 718-721, 2011.

[4] T. Nikoubin, A. Baniasadi, F. Eslami, and K. Navi, "A New Cell Design Methodology for Balanced XOR-XNOR Circuits for Hybrid-CMOS Logic", *Journal of Low Power Electronics*, Vol. 5, No. 4, pp. 474-483, 2009.

[5] T. Nikoubin, M. Grailoo, and S. H. Mozafari, "Cell Design Methodology based on Transmission Gate for Low-Power High-Speed Balanced XOR- XNOR Circuits in Hybrid-CMOS Logic Style", *Journal of Low Power Electronics*, Vol. 6, No. 4, pp. 503-512, 2010.

[6] Tooraj Nikoubin, Mahdieh Grailoo and Changzhi Li, "Energy and Area Efficient Three-Input XOR/XNORs with Systematic Cell Design Methodology", *IEEE Transactions on Very Large Scale Integration Systems*, Vol.24, No. 1, pp. 398-402, 2016.