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Three-Points Modulator Based on DPLL for Wideband Polar Modulation

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ABSTRACT

We present a nonlinear event-driven model of a Digital PLL used in the context of a polar modulation. This modeling has shown that the estimation method of the TDC gain has a big impact on the EVM for wideband modulation and a solution has been proposed which consists to add the modulation on the gain after calibration of the gain offset. This transforms the classical two-points modulator into a three-points modulator. This implementation has been validated for WCDMA standard.

Keywords: DPLL; Polar Modulation; WCDMA; TDC

1. Introduction

The number of wireless standards has expanded during the last decade, allowing the use of new applications such as internet for mobile or video calls for example. These new functions are very demanding in terms of debit rate. New communications standards have been developed to follow this evolution such as WCDMA and LTE for mobile phone. Their requirements in terms of noises, spurious, consumption, etc. are more and more stringent and their bandwidths more and more wider. In this context, the polar transmitter as shown in **Figure 1** seems to be an attractive architecture to reach these tough specifications.

The typical IQ signal, produced by the modulator, is converted by a Coordinate Rotation Digital Computer (CORDIC) into a polar signal. Lots of studies of the amplitude modulation by the Power Amplifier (PA) can be found in the literature[1,2], but the phase modulation by the PLL, which could be either analog or digital, seems to be less studied, especially for wideband modulations. This will be the core of this work.

In order to study the phase path, the modeling of the PLL has to be even more and more accurate. Many frequency-domain models have been developed in the past years from the classic Laplace model which can be used to study transfer functions and PLL noises to more complex sampled models [3-5] which are now very useful for the study of polar modulation. The model of Digital PLL proposed in this paper allows even more precision in the modeling of the different blocks of the PLL by including noises and nonlinearities and still allows fast simulation because it is event driven.

As already said, the main application for which our model has been developed is to observe the impact of a modulation passing directly through the PLL in the case of a polar modulation.

e-point modulator can be used for narrowband modulations, where the bandwidth is lower than the PLL cut-off frequency. The modulation is transmitted by adding the modulation data to the PLL frequency command word. Meanwhile, modulation bandwidth can be slightly enlarged by using a pre-distortion filter which compensates the PLL low path filtering [8]. However, PLL filtering and pre-distortion transfer function fitting mismatches limit the modulation bandwidth extension. Several methods for reducing the modulation bandwidth have also been proposed.

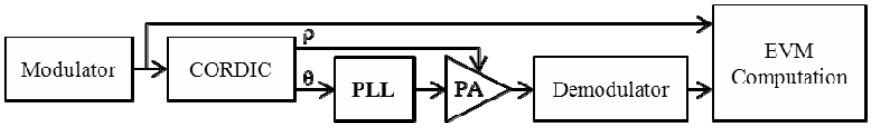

Figure 1. Polar transmitter.

On thus, for wideband modulations, two-point modulator [9] is necessary in order to release constraints due to PLL bandwidth and to remove pre-distortion filter. To go beyond PLL low path filtering, the modulation can be sent directly to the PLL output. Meanwhile, the modulation still has to be added to the PLL control word to avoid the loop feedback high pass filtering. This two point modulation reduces the impact of the PLL cutoff frequency on the modulation bandwidth.

This paper describes the proposed Digital PLL architecture model which underlines the necessity of 3 point modulation.

2. Digital PLL Time-Model

A simplified block diagram of a DPLL [6] on which our model is based is shown on **Figure 2**.

The PLL output frequency is defined by

$$f_{dco}[i] = (N + f).f_{ref} + f_{\mathrm{mod}}[i] \qquad (1)$$

where N and f are respectively the integer and the fractional part of the division ratio between the output frequency corresponding to the addressed channel and the reference frequencyf_{ref} and f_{mod} the eventual modulation frequency.

f_{dco} is generated by a Digitally Controlled Oscillator (DCO) from a command word (*Cmd*). A Frequency-Meter (FM) allows the conversion from the analog to the digital world, where the comparison between the wanted word, $N+f$, and the measured word, $N+f|_m$ is made. The intensive digital architecture allows the implementation of a digital loop filter.

Firstly, the model is described with the PLL used at first only as a frequency synthesizer.

2.1. Model Explanation

The proposed time-model is event-driven. Its efficiency comes by the limited number of calculation points, which allows reducing the simulation duration and the size of the database. So it simplifies the FFT for the phase noise analysis. Thus, the computations are done only for the useful edges: at least reference and DCO edges as shown on the chronogram on **Figure 3**.This allows fast simulations (about 50 µs/s of simulation in Matlab).

The chronogram describes the succession of phase displacement Δt which is related to the fractional part of the frequency ratio. The main equation governing the PLL behavioris:

$$\Delta t[i+1] = \Delta t[i] + N_{cpt}[i]T_{dco}[i] - T_{ref} \qquad (2)$$

where N_{cpt} is the number of DCO periods between two rising edges of the reference which is given by a counter. The fractional residue Δt is measured by a Time to Digital Converter (TDC).

2.1.1. TDC

In reality, the delay between the reference edge and the following DCO edge is quantized by a TDCif a precision better than more or less half a period of DCO is required.Several types of TDC exist in the literature; each one of them presents nonlinearities due to the analog-to-digital conversion. This represents the strongest nonlinearity in the loop. The TDC outputs two digital words corresponding to the phase displacement and the number *k*of quantization steps $T_q$over a DCO period as shown on **Figure 4**.

The digitized phase displacement can here be modeledas the integer part of the following ratio:

$$M[i] = \frac{\Delta t[i]}{T_q} \qquad (3)$$

Then, the equation (2) is replaced by:

$$T_{ref} = N_{cpt}[i]T_{dco}[i] + \left(M[i] - M[i+1]\right)T_q \qquad (4)$$

An estimation of the TDC gain, here called *k*, is requiredto get back to the T_{ref}/T_{dco} frequency ratio.

$$k[i] = \frac{T_{dco}[i]}{T_q} \qquad (5)$$

This measurement method is impacted by a quantization error so that a better precision can be achieved by filtering. Finally, equation (4) can be rewritten and gives the digital word corresponding to the frequency ratio:

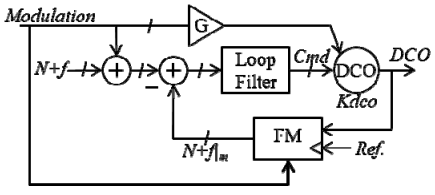

Figure 2. Three-points modulator based on digital PLL.

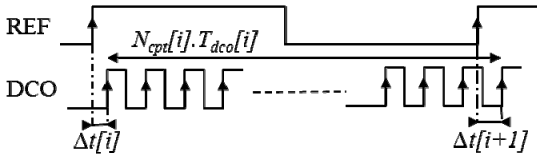

Figure 3. Chronogram.

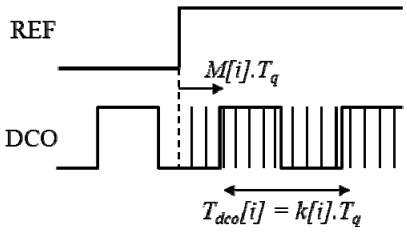

Figure 4. TDC inputs/outputs.

$$f_{dco}[i] = \left(N_{cpt}[i] + \frac{M[i] - M[i+1]}{k[i]} \right) f_{ref} \qquad (6)$$

2.1.2. Oscillator

A linear model of the DCO is as follow:

$$f_{dco}[i] = f_o + K_{dco} * Cmd[i] \qquad (7)$$

where f_o is the carrier frequency, K_{dco} the DCO gain and *Cmd* the digital command word.

DCO nonlinearity can also be modeled by replacing in (7) K_{dco} by a command word dependent-function K_{dco} (*Cmd*).

2.2. Noise Integration

The DCO and the reference signal noises profiles are based on circuit level simulation or measurement results. These are converted in time domain by an IFFT before adding these noises in our models as shown on **Figure 5**.

By slightly modifying (7), the next equation shows an easy way to inject DCO noise into the model:

$$f_{dco}[ki] = f_o + K_{dco} * Cmd[i] + dco_{noise}[i] \qquad (8)$$

where $dco_{noise}[i]$ corresponds to the instantaneous DCO frequency deviation in accordance with the DCO phase noise spectral density.

For the reference noise, equation (2) is modified in the same way. Adding a dither on the reference may be needed in order to break limit cycles due to TDC nonlinearities and then remove the spurs due to them as shown on **Figure 6**.

Without reference dithering (in black), the output phase noise presents a lot of spurious. Adding a dither, which corresponds directly to a calculus in our model, allows finding a match between the phase noise obtained with the formula proposed by Staszewski [7] for the TDC resolution effect on phase noise used for Laplace model (in dash) and the one obtained with our model (in grey).

3. Three-points Modulator

Figure 7 shows the impact on WCDMA constellations of a TDC gain either ideal, but with PLL noises (**Figure 7(a)**) or truncated (**Figure 7(b)**) as equation (5) or after filtering (**Figure 7(c)**), when the rest of the PLL is considered noiseless.

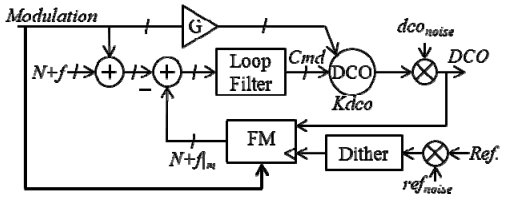

Figure 5. Digital PLL with noises.

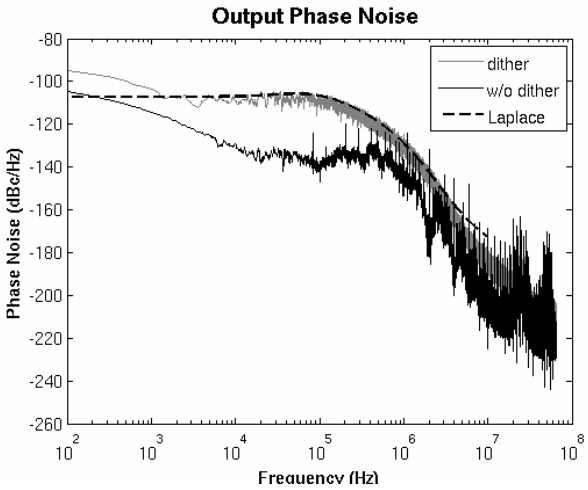

Figure 6. Output phase noise due to TDC quantization and dither.

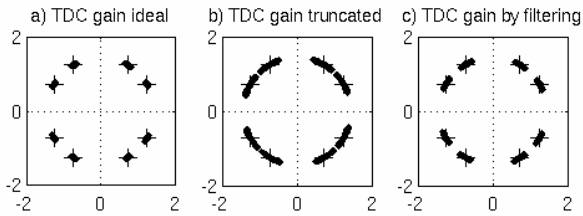

Figure 7. Impact of the TDC gain estimation on WCDMA constellation.

With an ideal TDC gain and the PLL imperfections, the EVMrms is about 2%. But if equation (5) is applied to obtain the TDC gain during the modulation frame, EVMrms is degraded up to by 14%. Adding filtering on the gain allows a good reduction of the EVM degradation depending of the bandwidth of this filtering, but still too important compared to the impact of the PLL noises. This shows that the classical measurement method with filtering cannot work for wideband modulations.

In synthesis mode, the output frequency is locked to $(N+f)f_{ref}$, so the TDC gain *k* defined in (5) tends to a constant value. By replacing $T_{dco}[i]$ by its value in synthesis mode, the final TDC gain obtained after filtering is:

$$k_{syn} = \frac{1}{(N+f) f_{ref} . T_q} \qquad (9)$$

In polar modulation mode, the instantaneous DCO period cannot be considered as constant anymore, at least for wide bandwidth. Looking back on the expression of the TDC gain defined previously, the equation (5) becomes:

$$k[i] = k_{syn} \frac{1}{1 + \frac{f_{\mathrm{mod}}[i]}{(N+f) f_{ref}}} \qquad (10)$$

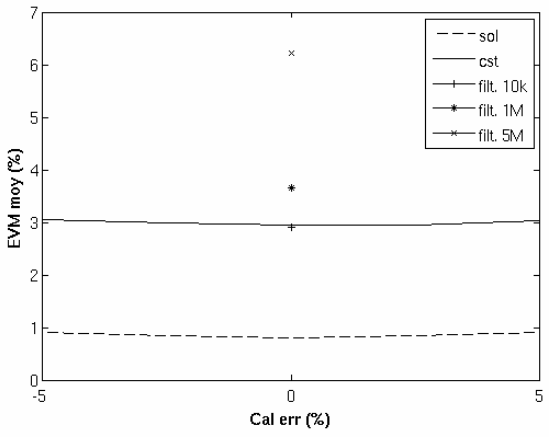

Figure 8. Impact of the different methods on EVM.

where k_{syn} is still the TDC gain in the synthesis mode defined in equation (10) and which is now calibrated before inserting the modulation into the PLL. Then, the modulation, normalized by the wanted output frequency, is applied on the TDC gain at each sample. This is the third inputs of the proposed three-points modulator.

The **Figure 8** shows the amelioration of the EVM with the implementation of this new expression instead of keeping the TDC gain filtered or constant after calibration. The PLL is still considered perfect.

Several observations can be made thanks to this figure. At first, it is useless to increase the TDC gain filtering bandwidth so that most of the modulation can pass without alterations. On the contrary, the EVM increases with the bandwidth enlargement.

Then, the proposed solution allows an EVM reduction of 2% compared to a method where the TDC gain is kept constant after the same calibration (filtering with 10 kHz-bandwidth in this case). Moreover, the solution presents certain robustness regarding a calibration error. In others words, having an offset on the gain estimation has less impact on EVM than not adding the modulation.The final EVM is under 1%, below the EVM with the rest of the PLL imperfections.

4. Conclusions

A nonlinear Digital PLL model has been developed to bring out the impact of TDC gain estimation in polar architectures. This causes indeed a large EVM degradation for wideband modulations such as WCDMA. The proposed solution which finally amounts to add the modulation on the TDC gain transforms the classical two-points modulator in a three-points modulator and allows a good reduction of the EVM degradation due to this contributor. This shows that the phase path is not straightforward for wideband modulations from the conclusions derived from GMSK/EDGE polar modulator.

5. Acknowledgements

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